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Design and Implementation of Positive Feedback Comparator In Terms of Power and Delay

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Abstract: *In this brief, a new positive feedback comparator design is proposed. The comparator plays an important role in the electronic circuits and these are used to compare two input signals and to produce the one output signal.*

A low-power two stage dynamic comparator is an advanced comparator and it contains PMOS transistors are used at the input of the first and second stages of the comparator. It reduces the power consumption by a factor of two, to achieve a controllable pre-amplifier gain. This comparator leads to increase in delay and transistor count. To overcome this problem a positive feedback comparator is proposed. This Positive feedback comparator is having lower power consumption and less propagation delay compared to existing low power two stage dynamic comparator. The backend simulations are achieved by using MENTOR GRAPHICS in 130nm technology and frontend simulations are done by using XILINX.

Keywords: *Pre-amplifier gain, Dynamic comparator, Low-power two stage dynamic comparator, Positive feedback comparator, Mentor graphics, Xilinx.*

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I. Introduction

Nowadays, ADCs are being used in a huge range of applications such as communication systems, biomedical implants, and digitally assisted analog circuits. Needless to say, comparators are one of the most effective blocks of commonly used ADCs such as Flash, SAR, and Pipeline ADCs. Operational Amplifiers were used in the past as static comparators [1]. Op-Amps suffer from a limited speed (because of the feedback and stabilization) and large amount of power consumption, since the circuit is always active because of small intrinsic gain of the transistors and short channel effects [2]. To overcome the problems of the static comparators, dynamic comparators were introduced [3,4]. In these circuits, a pre-amplifier stage is used to make a differential voltage based on the input differential voltage, then the latch is used to amplify the differential voltage generated by the pre-amplifier to the level of supply voltages (vdd and gnd). In these comparators the pre-amplifier and the latch outputs are directly connected together, therefore, the large swing generated by the latch is coupled into the input pins of the comparators through Gate-Drain capacitors (CGD) [5]. This effect is called kickback noise and it makes the usage of the comparators difficult in applications where a capacitive Digital to Analog Converter (DAC) is connected to the input pins of the comparator. In fact, the kickback noise distorts the voltage stored on the capacitors so cause non-linear errors in an ADC. In order to reduce the effect of the kickback noise, two-stage dynamic comparators were proposed [5]. In these comparators, the outputs of the pre-amplifier stage are connected to the latch inputs (the gate of the input transistors of the latch). Thus, the capacitive path from the latch outputs to the inputs is a series combination of two Gate-Drain capacitors (one for the pre-amplifier and one for the latch). Typically, the Gate-Drain capacitors of the latch are much smaller than that in the pre-amplifier, therefore, the kickback noise is reduced significantly. In the dynamic comparators both the clock and its inverted signal (*clkn=clk*) are necessary to perform the comparison. Although the comparator is a two-stage comparator, it suffers from the kickback noise because of the direct connection of the pre-amplifier and the latch stages. A low-power method is proposed which reduces the power consumption significantly but this comparator leads to increase in delay and transistor count. To overcome those problems a new method has been proposed named as "Positive feedback comparator". This Positive feedback comparator is having lower power consumption and less propagation delay compared to low power two stage dynamic comparators.

II. Comparator circuits

2.1Two stage dynamic comparator:

The two stage dynamic comparator and its equivalent circuit at the reset and evaluation phases as shown in fig 1.The input signals are connected to the pre-amplifier stage, and the outputs of the preamplifier stage are connected to the inputs of the latch stage. The functionality of this comparator is briefly described as follows. At the first phase, the reset-phase, the clk signal is "1" and clkn signal (the invert of clk) is "0". In this phase, the output voltages of the preamplifier stage are reset to gnd while the output voltages of the latch are reset to vdd. Fig. 1(b) presents the comparator at the reset-phase. "off" transistors are shown using grey color. Then to begin the evaluation-phase, clk is changed to "0" and clkn is changed to "1"; in fact, the constant paths to gnd and vdd are disconnected, respectively; also, the pre-amplifier current source (M5 in Fig. 1) is turned "on". Gradually, a differential voltage appears at the output nodes of the first stage. When the output voltage levels of the pre-amplifier stage become larger than the threshold voltage of the input NMOS transistor of the latch stage (M10 and M11 in Fig.1) the latch starts to amplify its input differential signal (using the positive feedback) to vdd at one side and gnd at the other side. And the outputs of pre-amplifier stage are vdd.

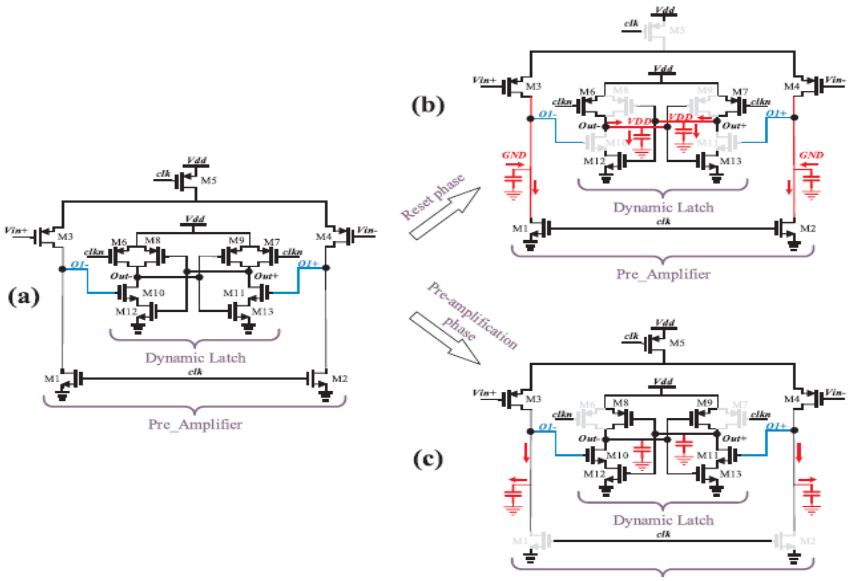

Fig. 1 (a)Two stage dynamic comparator (b) equivalent circuit during the reset phase (c) equivalent circuit during the evaluation phase.

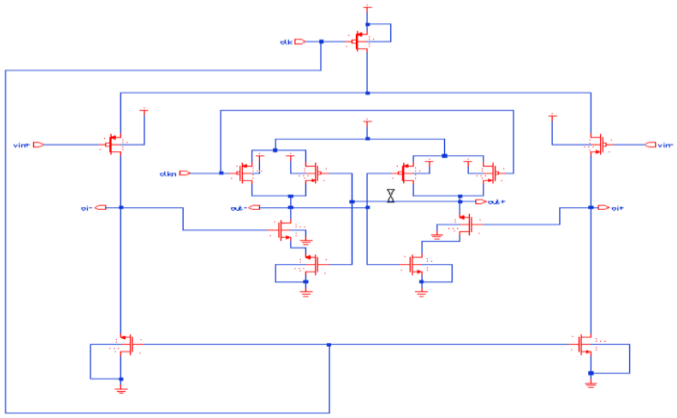

Fig. 2 Two stage dynamic comparator schematic diagram

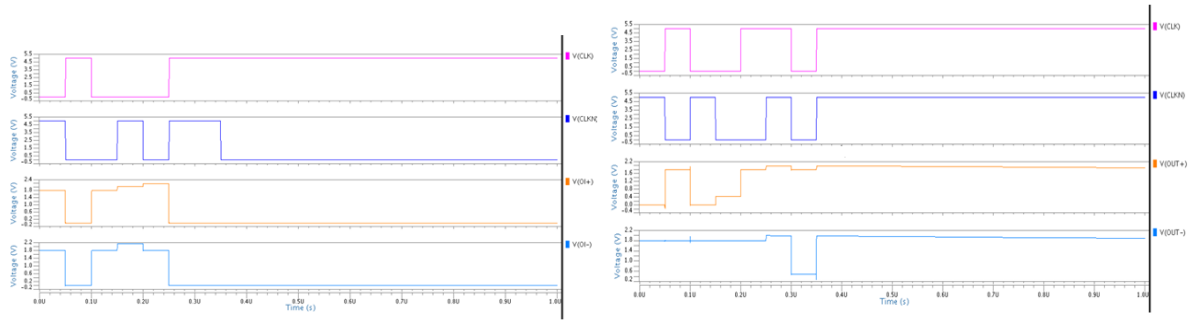

Fig. 3 Two stage dynamic comparator simulation results

2.2 Low-power Two stage dynamic comparator

In two stage dynamic comparator during the evaluation phase, the outputs of the pre-amplifier stage is increased from zero toward vdd. The charging process of the output nodes of the pre-amplifier stage continues. This phenomenon causes excess power consumption in the pre-amplifier stage which is the dominant stage in the total power consumption. The excess power consumption cannot be avoided because of the unknown delay of the comparator. To avoid those problem by using low-power two stage dynamic comparator.

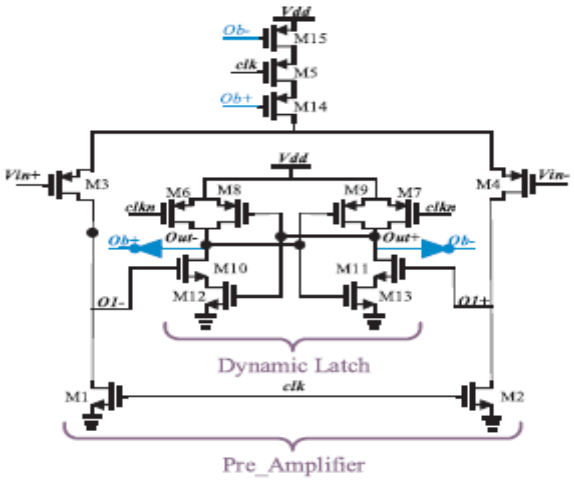

Fig. 4. Low-power two stage dynamic comparator

The low-power two stage dynamic comparator in addition to the output buffers are shown in above Fig.4. The structure of the comparator is similar to the two stage dynamic comparator. The output buffers are connected to PMOS transistors which are in series with the current source (M5). The reset and the evaluation phases of this comparator is the same as that of the conventional circuit. The additional transistors (M14, M15) are employed to prevent the excess power. In fact, when the voltage level of only one of the output buffers reaches to a level close to vdd, the current source of the pre-amplifier stage is turned "off" preventing the excess power. Thus, turning "off" the pre-amplifier stage has no effect on the dynamic behaviour of the comparator. Totally, the prevention from excess power consumption is achieved without any bad effect on the other parameters of the comparator. The series arrangement of M5, M14, M15 is not important regarding the functionality.

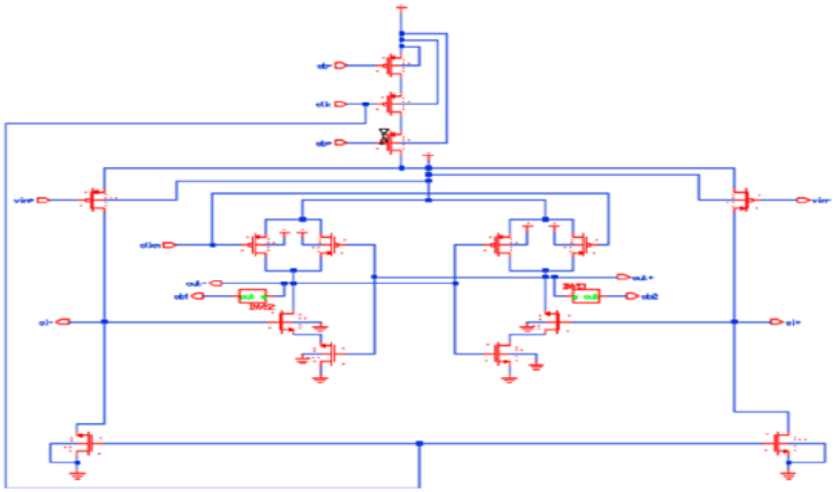

Fig.5 Low –power two stage dynamic comparator schematic diagram

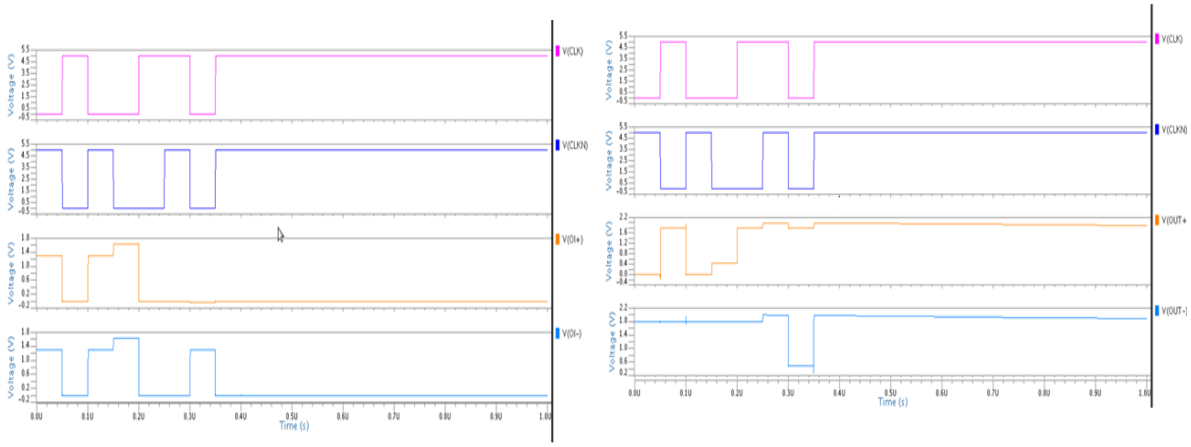

Fig.6 Low –power two stage dynamic comparator simulation results

2.3 The equivalent circuit of the low-power two stage comparator during the pre-amplification process

The below fig 6 represents the Equivalent circuit of proposed comparator during the pre-amplification phase, the output parasitic capacitors of the preamplifier stage are being charged from zero toward vdd. The charging rate of v_{oi+} and v_{oi-} are almost the same ($dV_{C1}/dt = dV_{C2}/dt$) during the pre-amplification process. Therefore, the power consumption of the pre-amplifier stage is calculated as follows (Vsupply=Vs, Isupply =Is).

$$\text{Power} = 1/T \int_0^T V_s \times I_s \, dt$$

$$= 1/T \int_0^T VDD \times (I_1+I_2)dt \,, \; dV_{C1}/dt = dV_{C2}/dt$$

$$I_{1,2} = C dV_{C1,C2}/dt$$

$$\text{Power} = 1/T \int_0^T VDD \times 2\, C dV_{C1,C2}/dt \, dt = 1/T \int_{V0}^{V1} VDD \times 2C dV_{C1C2}$$

$V_0=0$, $V1=V_{final}$

$P=2C/T \times VDD \times V_{final}$, $1/T = f$,

$Power=2C \times VDD \times V_{final} \times f$

Where V_{final} is the voltage stored over C, at the end of the conversion and f is the clock frequency. As discussed earlier, in the conventional comparator, Vfinal=vdd, however, in the proposed comparator V_{final} is less than vdd (e.g., 1.3 V in Fig 6). The power reduction of the proposed method is calculated as follows.

$$P_{conventional} = 2C/T \times VDD \times VDD = 2C/T \times VDD^2 = 2C \times VDD^2 \times f$$

$$P_{proposed} = 2C/T \times VDD \times V_{final} = 2C \times VDD \times V_{final} \times f$$

$$\text{Power reduction} = 1 - P_{proposed}/P_{conventional} = 1 - V_{final}/VDD$$

$$= (VDD - V_{final}) / VDD$$

The above fig 5 VDD=1.8 and V_{final} = 1.3 then the value of power reduction is

$$\text{Power reduction}(\%) = 100 \times (VDD - V_{final}) / VDD$$

$$= 100 \times (1.8-1.3)/1.8 = 27.7\%$$

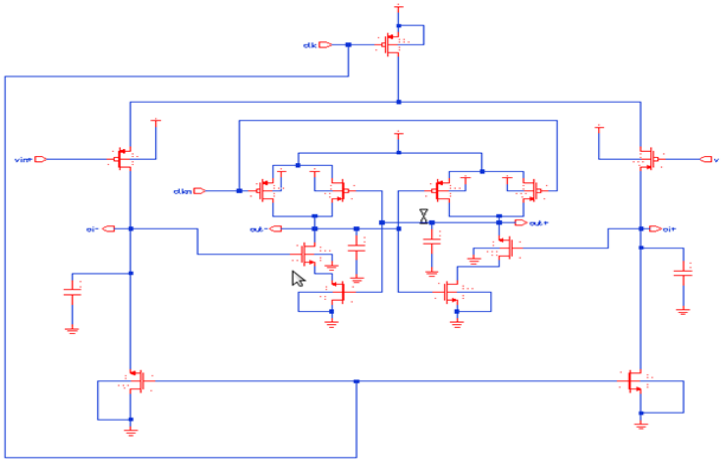

Fig 7. Equivalent circuit of the low-power two stage comparator during the pre-amplification process

III. System Overview

Here, in this method a positive feedback comparator design is proposed which is used to reduce the delay and transistor count compared to low-power two stage dynamic comparator.

3.1 Positive feedback comparator:

The operation of the Positive feedback comparator is as follows. During reset phase, both the tail transistors are in off state. When clock = 0, control transistors c1 and c2 are switched off. Transistors r1 and r2 resets the output to the ground. During the regeneration phase i.e vdd is equal to clock then both the transistors c1 and c2 are switched off. Transistors r1 and r2 resets the output to the ground. According to the input voltages the nodes fn and fp starts to discharge. If input (INP>INN), then node fn drops faster than fp, this makes the control transistor c1 to turn on, pulls fp backs to the vdd. This makes the node fn to discharge completely while other control transistor c2remains in off state.

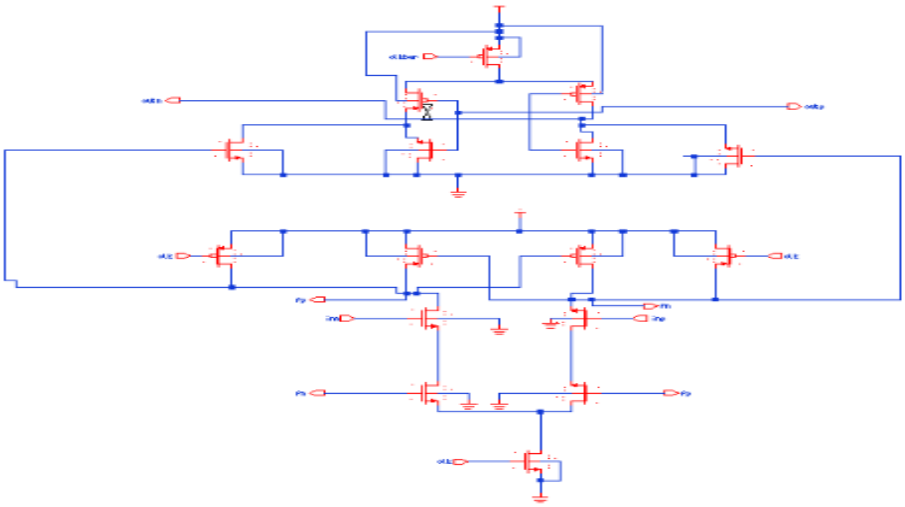

Fig 8. Positive feedback comparator schematic diagram

When (INN>INP) the operation is vice versa. Here node fp drops faster than node fn, this makes the control transistor c2 to turn on, pulls fn backs to the vdd. This makes node fp to discharge completely while other control transistor c1 remains in off state. The important factor to be noted is that, when one of the control transistors is in on state, this leads to flow of current from vdd to ground resulting in static power consumption. During the reset phase, pre-charging takes place from the node to vdd in which both the switching transistors are closed. During evaluation phase one of the nodes is discharge according to the input voltage and the control transistors detect the node which in turn speeds up the discharge rate. Hence, switching transistor closes the other side of the node and allows the discharge without any static power consumption.

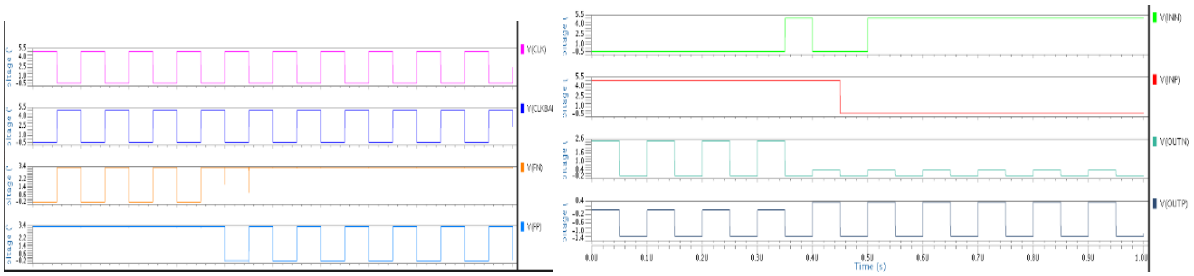

Fig 9. Positive feedback comparator simulation results

IV. Simulation Results

Power and Delay Comparision table

Parameter	Two stage dynamic comparator	Low power two stage dynamic comparator	Positive feedback comparator
Power (µW)	0.11 µW	0.005 µW	0.0005µW
Delay(ps)	291.36ps	414.53ps	100ps
No.of transistors	13	19	16

Xilinx results:

Positive feedback comparator:

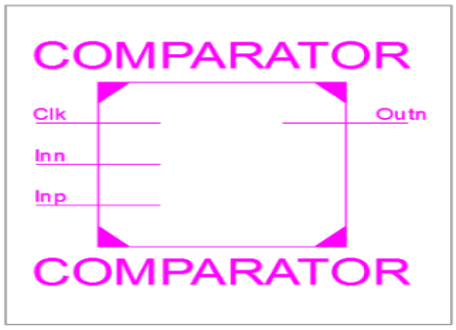

Fig 10.RTL schematic 1

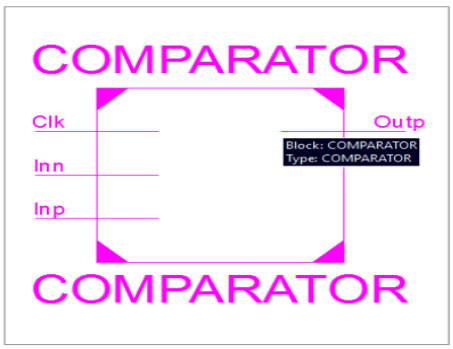

Fig11.RTL schematic 2

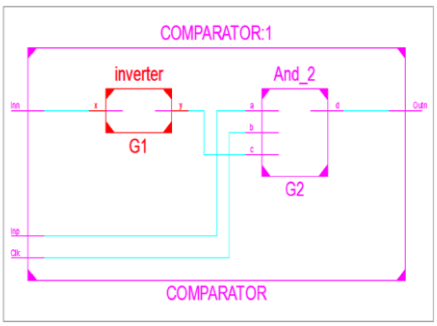

Fig 12. Internal RTL schematic 1

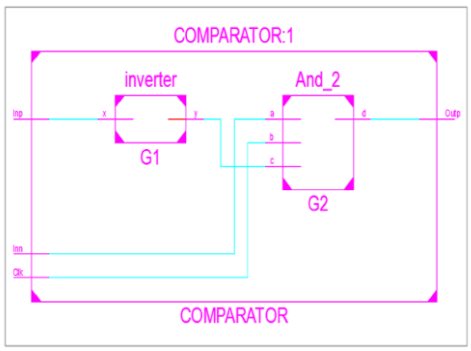

Fig 13. Internal RTL schematic 2

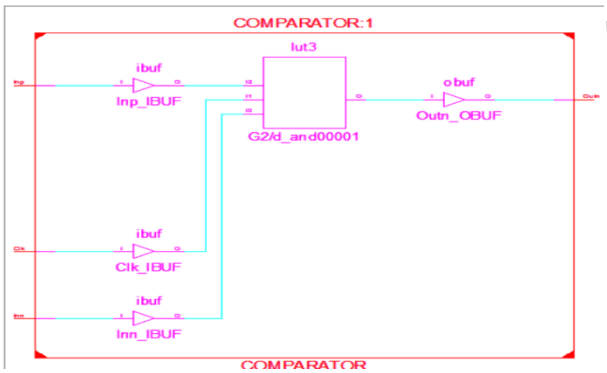

Fig 14. View Technology Schematic 1

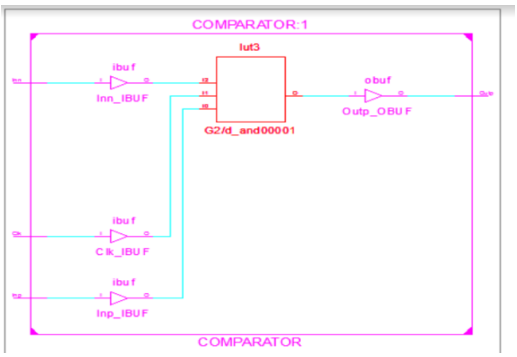

Fig 15. View Technology Schematic 2

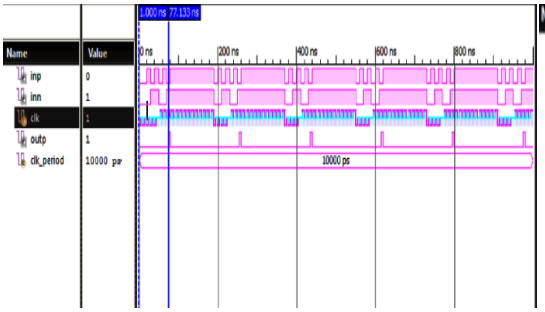

Fig 16. Timing Diagram1

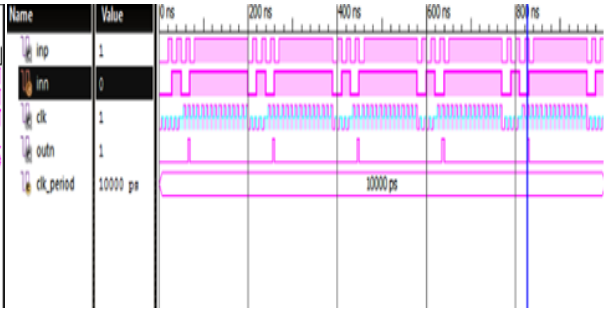

Fig 17. Timing Diagram2

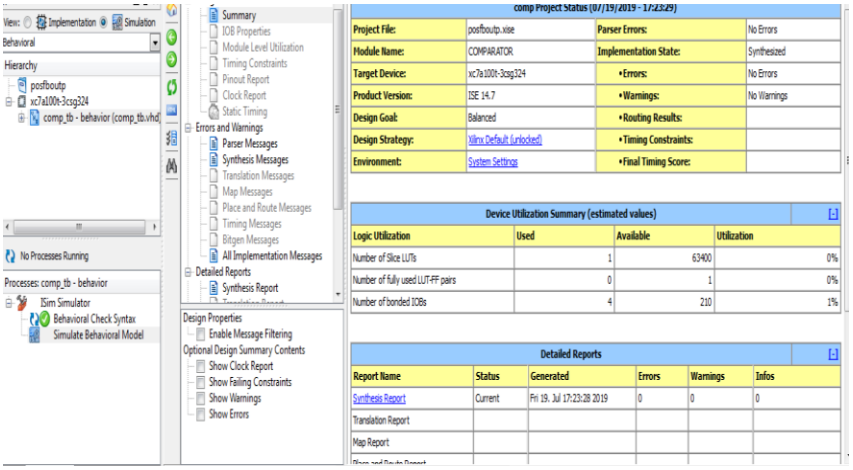

Fig 18. Summary report

V. Conclusion and Future scope

In this brief, a positive feedback comparator is proposed. This comparator is used to test circuit applications which can be used in ADCS, Flash, SAR and Pipelined ADCS. This type of comparator is used to achieve higher speed and reduces power. From simulation results one can design low power circuits and also can identify the performance improvement. For the study of hysteresis kick back noise should be minimized. On an average the future work can be any one among these. Accuracy(dynamic and static offset, noise, resolution), Settling time (tracking BW, regeneration speed), Sensitivity/resolution (gain), Meta stability.

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