IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 9, Issue 6, Ser. I (Nov. - Dec. 2019), PP 01-08
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design and Analysis of Low Power Fixed-Width Multiplier Using Reduced Precision Redundancy Block (RPR)

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Abstract:*This paper suggests a low power fixed-width multiplier using a reduced precision redundancy unit (RPR) for VLSI signal processing applications. RPR consists of a reduced precision module and a full precision module. The result of the reduced precision is considered as the correct output when the source output computes falsely. The proposed RPR fixed-width multiplier can satisfy the demand for accuracy, area efficiency, processing speed, and low power consumption. The precision of the proposed multiplier will be enhanced by the RPR logic. The compensation bias consists of probability and statistics. To avoid the truncation error many types of rounding methods are employed. The proposed RPR fixed-width multiplier is installed in the FIR filter design for various signal processing applications. The detailed analysis of the suggested multiplier gives 30% power reduction and 46.54% area reduction as compared with the different techniques.*

Keywords: *Fixed-width Multiplier; Reduced Precision Replica; Probability statistics; Error approximation; FIR filter*

Date of Submission: 02-12-2019 Date of Acceptance: 18-12-2019

I. Introduction

In recent years the advanced technology provides many portable electronic devices. According to Moore's law, the size reducing is more and more powerful during this era. Meanwhile, the performance of the same electronic device should improve individually. The processing speed and power requirement are the most common bottleneck of the innovations. Signal processing is the origination of all creation of the electronic world. There are infinity applications of signal processing specifically in, audio processing, video processing, speech processing, digital synthesizer, speech recognition, telecommunication, biomedical engineering, Radar, Sonar, etc. The signal processing field can have many branches like analog signal processing, digital signal processing, Ocean signal processing, RADAR signal processing, Space image processing and so on. But the simple multiplier circuit is the core of the enormous signal processor. Because the whole processor unit involves the performance of the multiplier circuit. The designing of multiplier requires more hardware when the number of bits increased. Here play many kinds of multiplier designs to prevent the impact such as booth, Baugh-Wooley, Wallace tree, modified boot, etc. The latest improvement of the multiplier is the Fixed-width multiplier. Because it saves many areas by sacrificing the partial products. So the operation is much easier than the earlier design. Thus processing speed and power dissipation is enhanced. The truncation error is the one drawback of this multiplication process. But many compensation techniques have been applied to solve the problem by various researchers. For example, the researcher Swartz et al added correction constant to reduce the error [1]. He considerably reduced hardware components from 25 to 35 percent. Kidambi et al proposed probability statistics to compensate for the truncation error[2] and consumes 50 percent area. Again Swartz et al developed a variable or approximate correction method to minimize the error[3] and achieved a better results than correction constant technique. Swartz et al suggest another technology called symmetric correction that will reduce error effectively and achieves better hardware complexity[4]. This method was applicable to all number systems. In this paper, a novel method is proposed to have a compact and error-free fixed-width multiplier using Reduced Precision Replica (RPR). We built a single-precision floating point fixed-width multiplier with the proposed technology and improve its accuracy by probabilistic statistics analysis. The designed fixed-width multiplier implemented in the FIR filter for VLSI signal processing applications. This paper organized as follows. Section 2 describes the detail of the fixed-width multiplier and the concept of the reduced precision replica. Then the third section explains the proposed work and the fourth section illustrates the simulation results. Finally, the last chapter discusses the conclusion and future work.

II. Background Knowledge

Fixed-width Multiplier:

The fixed-width multiplier has the fixed number of output product bits as the input. The fig1 shows the general architecture of the fixed-width multiplier[5]. From the architecture, we understood that the partial products are classified into various sections. The leftmost columns represent as Most Significant Part (MSP)[6-8]. And the rightmost column refers to the Least Significant Part (LSP). The LSP part is further distributed as LSP_{major} and LSP_{minor} for the convenient computation of correction constant. The LSP_{major} considered the leftmost 'h' columns and the rest ($n_{eq} = n - h$) of the column denoted as Input Correction (IC). The Not Formed (NF) section is the truncated part of the multiplier for the fixed width of output the same as the input. So there is a slight error in the result. To resolve the error many error approximation schemes were enabled [9-10].

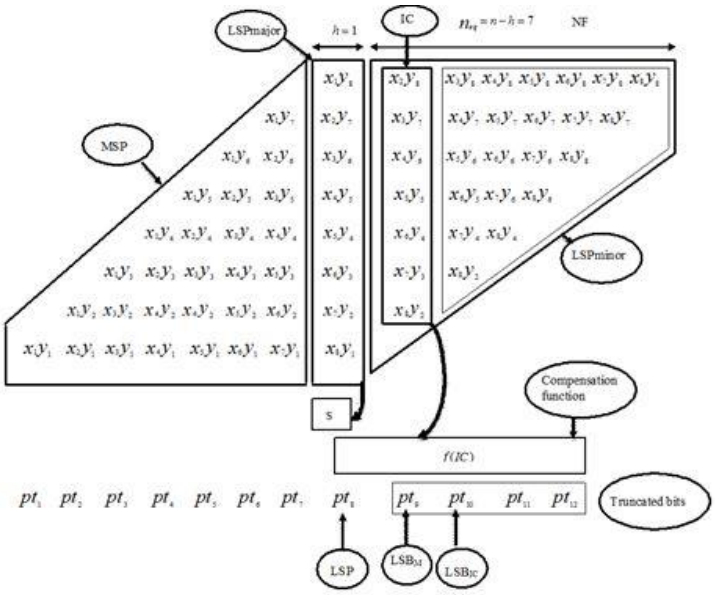

Figure no 1: The Architecture of Fixed-width multiplier for 8×8 matrix

$$P_{fw} = S_{MSP} + LSB\left\lfloor \frac{S_{LSB\ major} + f(IC)}{LSB} \right\rfloor (1)$$

Where S_{MSP} and S_{LSP} is the weighted sum of the MSP and LSP. The $S_{LSP\ major}$ is the weighted sum of the LSP major bits and the input correction function is denoted by f(IC).

Reduced Precision Replica (RPR):

This theory used to detect and correct the errors due to the truncation in the fixed-width multiplier. The truncation error occurs because of the elimination of the least significant bits (LSB). Though it causes major performance degradation, if we know the value of MSB, easily we can detect the error[16]. The RPR unit is a duplication of the actual partial product matrix with reduced precision operands. But the result from the RPR system provides small errors due to the loss of LSB data in the partial product matrix[18]. In case, the error was detected, the output of the RPR unit is acknowledged as actual output. The general architecture of the RPR System is shown in fig 2.

In paper [5] acknowledges the RPR technology is the most power-saving method. But it leads to performance loss due to the precision reduction. However, the RPR unit employed as an error reduction technique in the fixed-width multiplier, the performance achieves better in terms of power requirement and negligible precision loss. Even though this technique gives less power requirement and area overhead due to the missing elements of LSB bits, it can produce inexact output. Thereby causes deep degradation in the SNR output[20] So to recover the RPR system accuracy we employed LSB estimator. In the LSB estimator, the decision can be taken by the probability analysis.

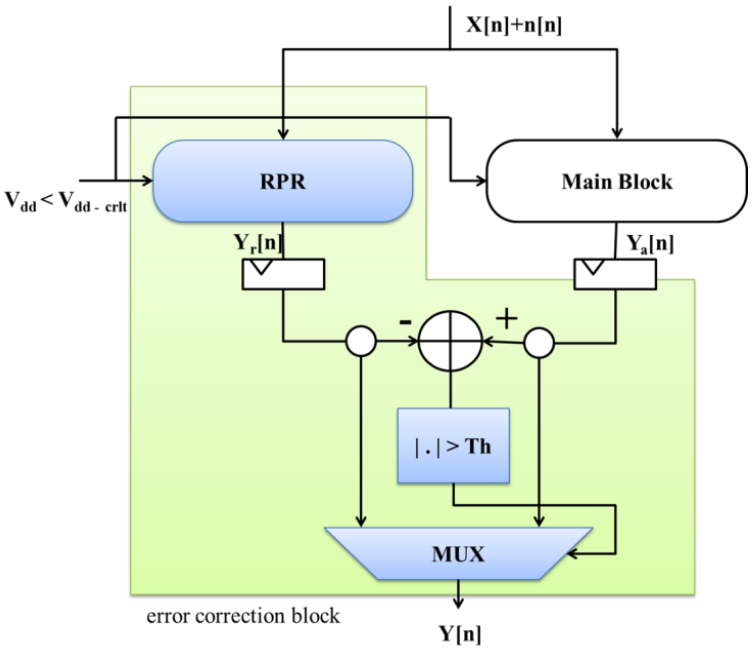

Figure no 2: The structure of Reduced Precision Replica (RPR) system

III. Proposed Work

FIR Filter using RPR System:

The unique RPR algorithm has been installed in the Fixed-width multiplier. The designed system achieves better performance in terms of area reduction and power reduction thereby realizes high processing speed. The proposed design has been employed in an FIR filter for performance evaluation. Figure 3 describes the Reduced Precision Redundancy (RPR) multiplier. The RPR system in the fixed-width multiplier used to reduce error and improves the SNR of the FIR filter response. Though the proposed design used to lessen the circuit complexity and power consumption, it also will increase the computation speed compared to the traditional fixed-width multiplier. But we have to compensate the huge difference in the output because of the elimination of the most LSB bits. The effective error reduction method follows probability, statistics, and linear regression analysis to find the approximate compensation function [19].

To consume circuit area overhead the compensation bias vector of the largest weighted bits of the LSB bits can directly be added to the result which does not want additional circuitry. To improve the accuracy of the multiplier, the proposed design will include the second most significant part of the compensation vector[17]. In this paper, we propose the input minor correction vector is the responsibility for the error correction. In other words, the error compensation circuit mainly consists of a minor input correction vector of the partial product matrix. The critical path delay will be reduced by placing the compensation circuit to the non-critical path delay area of the fixed-width RPR. Thus, the proposed design not only offers a high SNR ratio but also it reduced power consumption and area overhead [23].

The FIR filter architecture of the proposed RPR technique is illustrated in fig 3. The source system and the replica of the original system both use a multiply-accumulate (MAC) unit. The LSB estimator block has been added to the RPR system. This LSB estimator compensates for the data loss in the LSB of the partial product matrix. We considered a low pass FIR filter for simulation [22].

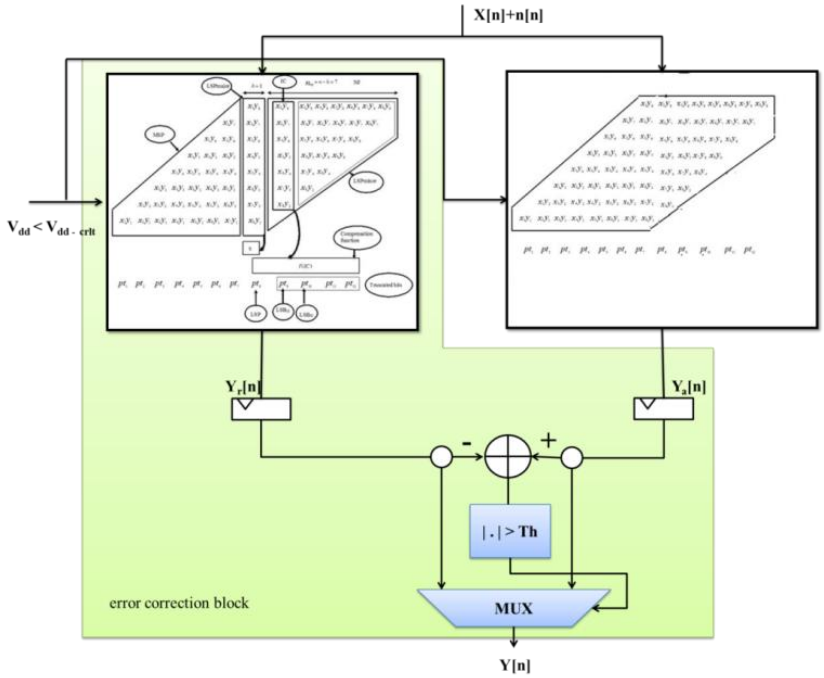

Figure no 3: The proposed architecture of the fixed-width multiplier

$$h[n] = \frac{\sin[\omega_c n]}{\pi n}.\omega[n] \quad (2)$$

Where $\omega[n]$ denotes symmetric N-point Hamming window function.

Let $y_o[n]$ is the output of the actual system and $y_r[n]$ denotes the output of the RPR system. The difference equation between both the system is derived as follows:

$$y_o[n] - y_r[n] = \sum_{k=0}^{N-1} h_o[k]x_o[n-k] - \sum_{k=0}^{N-1} h_r[k]x_r[n-k] \quad (3)$$

The filter coefficients and input error terms will be, $h_e = h_o - h_r$ and $x_e = x_o - x_r$

$$y_o[n] - y_r[n] = \sum_{k=0}^{N-1} h_e[k]x_o[n-k] + \sum_{k=0}^{N-1} h_r[k]x_r[n-k] \quad (4)$$

Suppose no error occurs in the operation, the above equation (4) is the normalization output of the RPR system. Hence, this differential equation can be used as a reference for error detection. So the absolute result can be explained by the probability analysis as,

$$|y_o[n] - y_r[n]| \leq T \quad (5)$$

Where T is a threshold given by,

$$T = \sum_{k=0}^{N-1}|h_e[k]|.\left|x_{o,max}[n-k]\right| + \sum_{k=0}^{N-1}|h_r[k]|.\left|x_{e,max}[n-k]\right| \quad (6)$$

The above-calculated bounding equation is obtained by the maximum number of inputs. So the selective of the correct threshold is much simpler. If the difference between the two systems is smaller than the threshold value, we consider there is no error or a negligible error was present. If the difference is higher than the threshold value, then there is an error present. In case of error detection, we consider the RPR output is the correct one. If not we use the actual output. The decision algorithm for selecting the correct output is given by,

$$y_n = \{y_o[n] \quad \text{if } d(y_e, y_r) \leq T, y_r[n] \text{ if } d(y_e, y_r) \quad (7)$$

Probabilistic Analysis of the LSB Estimator:

The Reduced Precision Replica (RPR) system has a limitation of having information loss due to the truncation of LSB of partial products. Though it offers a considerable amount of power and area reduction, it has a drawback of some accuracy loss. To avoid incorrect selection and error detection we implement LSB

estimator to compensate for the least significant partial products. The improved result of the RPR system with LSB estimator in [11-12],

$$y_r^{'} = y_r + \Delta \quad (8)$$

Where Δ is the LSB correction value. Let consider k-tap FIR filtering and the original and RPR system have n and l number of bits respectively. In two's complement multiplication, the actual product is expressed as

$$x_k . h_k = \left(-x_{k,n-1}2^{n-1} + \sum_{m=0}^{n-2} x_{k,m}\, 2^m\right).\left(-h_{k,n-1}2^{n-1} + \sum_{m=0}^{n-2} h_{k,m}\, 2^m\right) \quad (9)$$

And the multiplication product of the RPR system is given as,

$$x_k^r . h_k^r = \left(-x_{k,n-1}2^{n-1} + \sum_{m=n-l}^{n-2} x_{k,m}\, 2^m\right).\left(-h_{k,n-1}2^{n-1} + \sum_{m=n-l}^{n-2} h_{k,m}\, 2^m\right) \quad (10)$$

The operational error between both the system can be expressed as

$$\varepsilon \cong \sum_k [(-x_{n-1}\, 2^{k,n-1} + \sum_{m=n-l}^{n-2} x_{k,m}\, 2^m) \sum_{m=0}^{n-l-1} h_{k,m}\, 2^m + \sum_{m=0}^{n-l-1} x_{k,m}\, 2^m (-h_{k,n-1}2^{n-1} + \sum_{m=n-l}^{n-2} h_{k,m} 2^m] \quad (11)$$

The objective of the LSB estimator is to compensate for the missing elements in the LSB. In the case, of the distortion between lost LSB value and LSB estimator value is small, then there is improving output accuracy. The distortion is given by[13-15],

$$d^2(\varepsilon, \Delta_j) = \int \sum_{i=1}^{K} (\varepsilon_i - \Delta_j)^2 f_c(\varepsilon) d\varepsilon \; j = 1, \ldots . L \quad (12)$$

Where Δ_i is the $'i^{th}'$ element of the LSB estimator.

IV. Simulation Results and Discussion

In this segment, we analyzed the multiplier characteristics and the filter performance through MATLAB Simulink. The multiplier characteristics can be evaluated by their error performance and electrical performance [21]. The electrical performance consists of area, power and delay analysis. The filter performance can be measured with the help of the parameter called signal to noise (SNR) ratio. The computation and simulation results are discussed below.

The designed RPR fixed-width multiplier consists of two unsigned n-bit numbers expressed as,

$$X = \sum_{i=0}^{n-1} x_i 2^i, \quad Y = \sum_{j=0}^{n-1} y_j\, 2^j \quad (13)$$

The partial product matrix of x_i and y_j is known as the multiplication output of P.

$$P = \sum_{k=0}^{2n-1} P_k\, 2^k = \sum_{j=0}^{n-1} \sum_{i=0}^{n-1} x_i y_j 2^{i+j} \quad (14)$$

The result contains four parts namely MSP, ICV,MICV and LSP. The fixed-width multiplier eliminates all parts except the MSP. The truncated parts contribute to the largest weight of the product. So the truncated part is most important to construct the error compensation function. To compute the accuracy of the proposed design we find the variance among the source multiplier and the replica system,

$$\varepsilon = P - P_t \quad (15)$$

Where

$$P_t = \sum_{j=\frac{n}{2}+1}^{n-1} y_j\, 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i\, 2^i + f(EC) \quad (16)$$

The performance of the proposed design depends on electrical and error characteristics. For that, we considered system total error, signal to noise ratio, system power requirement and processing speed of the design. All the parameters were compared against various kinds of a largest weighted parameter calledβ. Based

on the discussion we identified which parameter could be better for the fixed-width RPR system. The analysis of the performance evaluation can be done by the graphical illustration as follows.

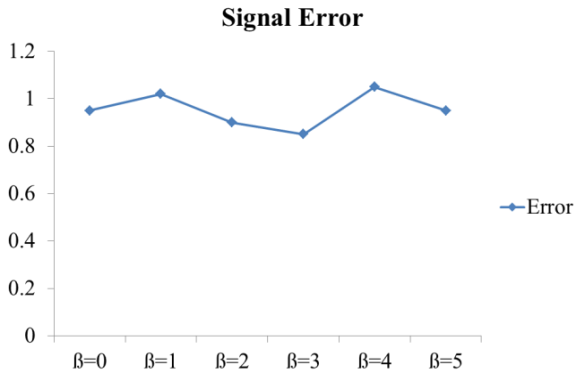

Figure no 4: The Graphical representation of the parameter β and the signal error

We analyzed the recommended fixed-width multiplier features by simulating the waveforms in the MATLAB tool. From fig 4 we gain knowledge about the association between the parameter β and the truncation error. The inaccuracy in the fixed-width multiplier with RPR can be controlled by the largest weighted numbers. Thus less cost compensation function circuit can be designed if we know the relationship between the error correction function and the parameter β. The parameter β is known as the summation of all the largest weight partial product bits. The average error statistically distributed between β and $\beta + 1$.As the graph indicates that there is a slight variation between $\beta = 0$ and $\beta + 1$. Likewise, the compensation vector of $\beta < 0$, there is close related vector values. So we can need only one compensation vector as an error estimation bias. Thereby we can directly include the compensation bias vector to the fixed-width RPR, it does not need an extra circuit. But in the case of absolute mean error, there will be less relation to the number of bits β. So multiple correction constant have to be added for the occurrence of the high precision results.

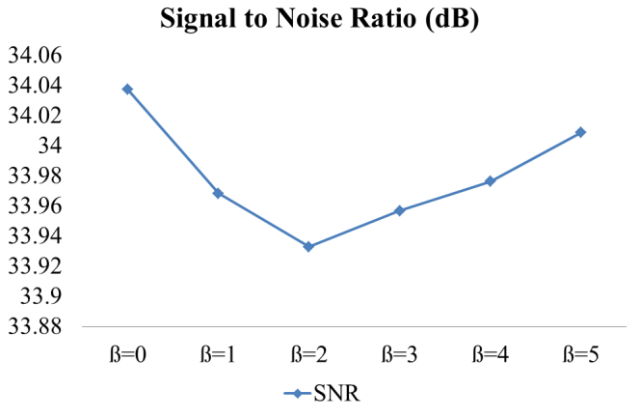

Figure no 5: The comparison between the parameter β and SNR

The proposed multiplier is implemented in the FIR filter for VLSI signal processing applications. To evaluate the filter performance we have to analyses the Signal to Noise (SNR) ratio. The term SNR is defined as the desired signal power to the noise power. The parameter SNR ratio will be high to get better performance. The desirable SNR value should be higher than 25dB. In fig 5 we are getting above 25dB for the parameter $\beta < 0$.From the graph we conclude that the good SNR result achieved when the probability of error is low. Because the signal to noise ratio depends on the system accuracy.

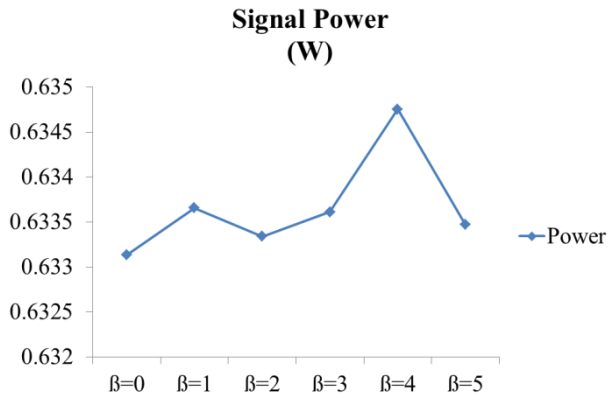

Figure no 6: Analysis of the power requirement

Power consumption is one of the significant parameter for the performance analysis. We know that the requirement of the power is proportional to circuit area. Since it reduces most of the LSB bits in the partial products, the circuit area will get smaller. Eventually, the constraint amount of power also will be decreased. Though the proposed design consists of the replica of the source multiplier, the required amount of power will incredibly lesser than any other RPR system. Figure 6 shows that the relation between the power intake of the proposed logic to the parameter β. Here, for the voltage supply at 0.623, the power can be lowered to 393 µW with 50% power saving.

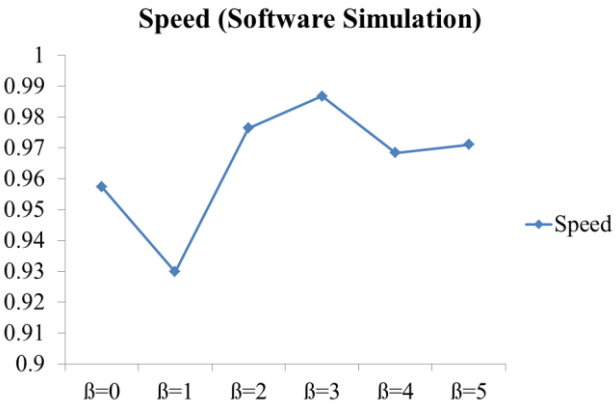

Figure no 7: Analysis of the computation speed

The processing speed is a very essential factor for the VLSI applications. The speed in other terms which is represented by delay is the inversely proportional relationship with each other. If delay is minimum, the computation time became fast. The proposed design, concerning for to the reduction in the partial product matrix, the processing speed became faster than before. Figure 7 provides the processing speed graph regarding various weight partial products. From the graph, we conclude that $\beta = 1$, the operational speed is high. Therefore many partial product bits truncated at $\beta = 1$. The delay is expressed in Nanoseconds. The minimum delay occurred as 0.93 ns.

V. Conclusion and Future Work

In this paper, a low error and high-speed floating-point fixed-width RPR based multiplier are designed and analyzed. Then the physiognomies of the designed fixed-width multiplier using the RPR system are investigated using MATLAB Simulink software. The graphical analyses of the error and electrical parameters have been noted. And then the proposed single-precision (32 bit) multiplier has been implemented in the FIR filter for signal processing application.We analyzed various kinds of parameters from the graphical depiction. For the error analysis, we have taken the parameter β and the number of errors. From the given graph we considered better accuracy when the largest weighted $\beta = 3$. So multiple correction constant have to be added for the occurrence of the high precision results. The next parameter will be the Signal to Noise ratio (SNR). The SNR is above 25dB for the parameter $\beta < 0$. From the graph, we conclude that the good SNR result achieved when the probability of error is low. The power requirement of the designed system is illustrated between different values for β. The consumption of power at $\beta = 0$ is 393 µW with 50% power saving. From the graph, we conclude that $\beta = 1$, the operational speed is high. The minimum delay occurred as 0.93 ns

The summary of the proposed design and the future scopewill be given as follows. The analysis of the FIR filter provides a desirable signal at an SNR of about 25dB. The total power requirement for the process is 393µW at 0.623V supply voltage and 200-MHZ operating frequency. Moreover, the presented design consumes a 45% circuit area by truncation. In the future, the suggested design can implement in the VLSI hardware kit for performance evaluation.

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JencyRubia J " Design and Analysis of Low Power Fixed-Width Multiplier Using Reduced Precision Redundancy Block (RPR)." IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) , vol. 9, no. 6, 2019, pp. 01-08.